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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/265,119	03/09/1999	MAURIZIO PERI	856063.579	4151

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
SHARON, AYAL I	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/265,119	PERI ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-20 of U.S. Application 09/265119 filed on 03/09/1999 are presented for examination. Foreign Priority filing date is 9/30/98.

Telephonic Interview Summary

2. On June 25, 2002, Examiner conducted a phone conversation with Applicant's representative, Robert Iannucci, No. 33514, because two IDS papers (paper #4 and paper #6) listed on the file wrapper of case 09/265,119, while only one IDS (labeled paper #6, but with the mailing date of paper #4) was found in the file wrapper. Mr. Iannucci informed the Examiner that only one IDS was mailed for the instant application, on Nov. 2, 1999. This corresponds to paper #4 on the file wrapper.

Preamble of the Claims

3. The preambles of Claims 1, 8, 10, and 16, as presented for examination, have not been given patentable weight. Appropriate weight is given to limitations recited in the body of the claim that are needed for purpose of antecedence. "A mere statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the

language of a preamble is necessary to give meaning to the claim" *Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987)*

Information Disclosure Statement

4. The Applicants are reminded of their declaration acknowledging the duty to disclose to the Office all information known to them to be material to patentability as defined in 37 CFR 1.56.

5. During the process of examination, Examiner has been made aware of the existence of the following related prior art, authored by one or more of the applicants:

   - Andretta, F., Peri, M., Pozzi, C. "Testing of the ST9 Microcontroller". Proceedings of the 20th EUROMICRO Conference, 1994. Sept. 5-8, 1994. pp.322-328.
   - "Onwards and Upwards: New developments in 8-bit Micros". Challenge: News and Views from STMicroelectronics, March 1999, p.2. The article says that: "Although it is possible to make part of the Flash memory look like EEPROM by means of software simulation, this approach does not ideal [sic] in embedded applications.For the ST9 and ST10 families, ST offers a unique, patented solution to this problem. The process used is also able to provide hardware emulation of EEPROM functionality ..."
   - Brigati et al., U.S. Patent 5,991,199.

- Brigati et al., U.S. Patent 6,011,717.
- Devin et al., U.S. Patent 6,141,254.
- Cappelletti et al., U.S. Patent 6,275,960.

6. Applicants are requested to provide the patents referred to in the "Onwards and Upwards" press release, which was contemporaneous with the instant application.
7. Moreover, Applicants are requested to provide specification sheets or data sheets for the versions of the ST9 Microcontroller produced in the years 1994-1997.
8. Applicants are requested to provide as all other patents and articles published by the applicants that may be material to patentability.

Oath/Declaration

9. During the process of examination, Examiner has been made aware of the existence of the following patents, authored by one or more of the applicants, that contain material relevant to the instant application:
   - Brigati et al., U.S. Patent 5,991,199.
   - Brigati et al., U.S. Patent 6,011,717.
   - Devin et al., U.S. Patent 6,141,254.
   - Cappelletti et al., U.S. Patent 6,275,960.
10. Clarification as to relationship of Misters Devin, Leconte, Demange, Aulas, Guedj, Cappelletti, and Maurelli to the claimed invention is requested.

Drawings

11. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

12. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Flash EEPROM Memory Emulator of Non-Flash EEPROM Device and Corresponding Method".

Claim Interpretations

13. Examiner interprets a "Flash" memory structure as being a "flash EEPROM" as described in Brigati et al., U.S. Patent 6,011,717, Col. 1, lines 24-31.
14. Examiner interprets "Flash EPROM" as being a set of devices that include "flash EEPROM".

Claim Objections

15. Claim 9 is objected to because of the following informalities: "... are swapped **to the another** ...." Should either be: "to another" or "to the other". Appropriate correction is required.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 1,8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 8 refer to a "predetermined number of sectors", however, this "predetermined number of sectors" is not specified. All dependent claims inherit this defect.

18. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 refers to "predetermined number of blocks" and "predetermined number of pages", however, these are not specified. All dependent claims inherit this defect.

19. The specification regarding the claimed invention is deficient in the areas cited above. Accordingly, the examiner has made prior art rejections based on the limited scope of information contained in the specification for supporting the claims. The rejections are complete and specifically applied against the claims based on this limited disclosure.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

21. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

22. The prior art used for these rejections is as follows:

- Brigati et al., U.S. Patent 5,991,199. (Henceforth referred to as "**Brigati**")

23. Claims 1-9, 16-17 and 19-20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.

24. Claim 1 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.

> 1. An emulated EEPROM memory device, comprising a memory macrocell which is embedded into an integrated circuit having a microcontroller, the memory macrocell including a Flash memory structure formed by a predetermined number of sectors, wherein at least two sectors of the Flash memory structure are structured to emulate EEPROM byte alterability.
> (Brigati: especially Fig.1-3 and Col.5, line 60 to Col.8, line 35)

25. In regards to Claim 2, the emulated EEPROM memory device according to claim 1, wherein said EEPROM byte alterability is emulated by hardware means, is taught by Brigati (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

26. In regards to Claim 3, the emulated EEPROM memory device according to claim 1, wherein 8 Kbyte of the Flash memory structure are used to emulate 1 Kbyte of an EEPROM memory portion, is taught by Brigati (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

27. In regards to Claim 4, the emulated EEPROM memory device according to claim 1, wherein first and second EEPROM emulated sectors are each divided in a pre-determined number of blocks of the same size and each block is divided in pages, is taught by Brigati (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

28. In regards to Claim 5, The emulated EEPROM memory device according to claim 1, wherein a state machine is provided for controlling an address counter which is output connected to an internal address bus running inside the memory macrocell, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update, is taught by Brigati (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

29. In regards to Claim 6, the emulated EEPROM memory device according to claim 5, wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase, is taught by Brigati. (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

30. In regards to Claim 7, the emulated EEPROM memory device according to claim 1, wherein Flash and EEPROM memories operations are controlled through a register interface mapped into the memory, is taught by Brigati (especially Fig.1-3 and Col.5, line 60 to Col.8, line 35).

31. Claim 8 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.

> 8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode.
> (Brigati: especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8)

32. In regards to Claim 9, the method according to claim 8, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector, is taught by Brigati (especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8).

33. Claim 16 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Brigati.

> 16. A method of emulating an EEPROM using Flash memory, the method comprising:
>
> dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;
> (Brigati: especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8)
>
> assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors;
> (Brigati: especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8)
>
> in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and
> (Brigati: especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8)
>
> in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.
> (Brigati: especially Fig.1-3 and Col.7, line 65 to Col.8, line 40 and Col. 11, line 62 to Col. 12, line 8)

34. In regards to Claim 17, the method of claim 16, further comprising, in response to a third write instruction to write to the selected page address when a most recent write instruction to write to the selected page address was executed by writing to a last memory block of the first memory sector, executing the third write instruction by writing to a first memory block of the second memory sector, is taught by Brigati (especially Col. 11, lines 42-65).

35. In regards to Claim 19, the method of claim 16, further comprising erasing the second memory sector while updating memory pages of the first memory sector,

is taught by Brigati (especially Col. 11, line 65 to Col.12, line 8, and Col. 12, lines 41-51).

36. In regards to Claim 20, the method of claim 19 wherein the erasing act is performed in plural erase phases, with each of the erase phases being triggered by writing data in the first memory sector, is taught by Brigati (especially Col. 11, line 65 to Col.12, line 8, and Col. 12, lines 41-51).

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. The prior art used for these rejections is as follows:

- Brigati et al., U.S. Patent 5,991,199. (Henceforth referred to as "**Brigati**")
- Devin et al., U.S. Patent 6,141,254. (Henceforth referred to as "**Devin**")
- Cappelletti et al., U.S. Patent 6,275,960. (Henceforth referred to as "**Cappelletti**").

39. Claims 10-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devin in view of Cappelletti.

40. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Devin in view of Cappelletti and further in view of Official Notice.

41. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brigati in view of Cappelletti.

42. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Devin in view of Cappelletti.

> 10. A Flash memory device for emulating an EEPROM, comprising:
>
> first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions. all of the memory locations sharing a same address being a set of memory locations; and
>
> a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and
>
> a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.

Devin teaches the use of a Flash memory device, and first and second memory portions for programming the device. However, Devin does not expressly teach the use of pointers for reading and writing to memory locations.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

43. In regards to Claim 11:

> 11. The Flash memory device of claim 10 wherein the first and second Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second Flash memory portion.

Devin teaches the use of a Flash memory device, and first and second memory portions for programming the device. However, Devin does not expressly teach the use of pointers.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

44. In regards to Claim 12:

> 12. The Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.

Devin teaches the use of a Flash memory device, and a plurality of memory portions for programming the device.

However, Devin does not expressly teach the use of pointers.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

45. In regards to Claim 13:

> 13. The Flash memory device of claim 12 wherein the plurality of Flash memory portions include two Flash memory portions, each with four memory blocks, each memory block including 64 memory pages each with 16 memory locations that are able to store a data byte.

Devin teaches the values of cell (M), word (N), and memory cell (P). (See Col. 9, lines 36-50, and Col. 10, lines 15-50). Devin also teaches the cases when M is not equal to 1 (See Col. 10, lines 17-20).

However, Devin does not expressly teach the values 4, 64, and 16. Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the values 4, 64, and 16 as the number of memory blocks, memory pages, and memory locations respectively, because these are base 2 values commonly used in the art.

46. In regards to Claim 14:

> 14. The Flash memory device of claim 10, further including a third Flash memory portion not organized to emulate the EEPROM.

Devin teaches the use of a Flash memory device, first and second memory portions for programming the device, and a third Flash memory portion not organized to emulate the EEPROM (Devin: especially Col. 1, lines 27-32).

However, Devin does not expressly teach the use of pointers for reading and writing to memory locations.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

47. In regards to Claim 15:

> 15. The Flash memory device of claim 14, further including first and second sense amplifiers, the first sense amplifier being coupled to, and structured to read, the first and second Flash memory portions and the second sense amplifier being coupled to, and structured to read, the third Flash memory portion.

Devin teaches the use of a Flash memory device, first and second memory portions for programming the device, and a third Flash memory portion not organized to emulate the EEPROM, and first and second sense amplifiers structured and coupled to read the third Flash memory portion (Devin: especially Col. 1, lines 27-32 and Col. 8, lines 58-67).

However, Devin does not expressly teach the use of pointers for reading and writing to memory locations.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

48. In regards to Claim 18:

> 18. The method of claim 16 wherein all memory pages sharing a same page address constitute a set of memory pages, the number of sets of memory pages equaling how many memory pages are in each memory block, the method further comprising:
>
> assigning to each set of memory pages of the first and second memory

sectors a page pointer that reflects which memory page in the set has been most recently updated; and

in response to each write instruction requesting to write data to the selected page address, determining which page pointer is associated with the selected page address, determining from the page pointer associated with the selected page address which memory page of the set of memory pages assigned the selected page address is next to be updated, and writing the data in the memory page that is determined to be the next memory page to be updated.

Brigati teaches the use of a Flash memory device, and the use of first and second memory pages for reading and writing (see Col. 11, lines 42-62). However, Brigati does not expressly teach the use of pointers.

Cappelletti does expressly teach the use of pointers when programming the memory portions of a Flash memory device (see Col.2, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Devin with Cappelletti because doing so optimizes the programming of Flash memory devices.

Conclusion

49. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

50. Andretta, F., Peri, M., Pozzi, C. "Testing of the ST9 Microcontroller". Proceedings of the 20th EUROMICRO Conference, 1994. Sept. 5-8, 1994. pp.322-328.

51. "Onwards and Upwards: New developments in 8-bit Micros". Challenge: News and Views from STMicroelectronics, March 1999.

52. Brown et al. "Simultaneous Code Execution and Data Storage in a Single Flash Memory Chip for Real Time Wireless Communication Systems". Proceedings of the 40th Midwest Symposium on Circuits and Systems, 1997. Aug. 3-6, 1997. pp. 740-745, vol. 2.

53. Nakamura et al. "An Intelligent Subprocessor for Hardware Emulation with 20-MOPS performance." IEEE Journal of Solid-State Circuits. Nov. 1991. Vol. 26, Issue 11. pp.1662-1668.

54. Robinson, U.S. Patent 5,937,423.

55. Sukegawa et al., U.S. Patent 5,603,001.

56. Cernea et al., U.S. Patent 5,508,971.

57. Wallace et al., U.S. Patent 5,663,901.

58. Cernea et al., U.S. Patent 5,596,532.

59. Akiyama et al., U.S. Patent 5,872,994.

60. Marsters, U.S. Patent 6,092,160.

61. Bothwell, U.S. Patent 5,912,848.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications:	(703) 746-7239
Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 28, 2002

William Thomson

Art Unit 2123

June 28, 2002